

CEDA Hardware Development Kit v2.9

Put your image-processing algorithm inside the GigaSens CV 2.0 CXP camera.
The full sensor rate - 2,247 fps at 1080p - processed before it ever hits the wire.

2,247 fps

1920 X 1080, 8-BIT OUT

CXP-12 x4

COAXPRESS / GENICAM

8 / 10-bit
OUTPUT, FROM A
10-BIT PIPELINE
109,418 fps

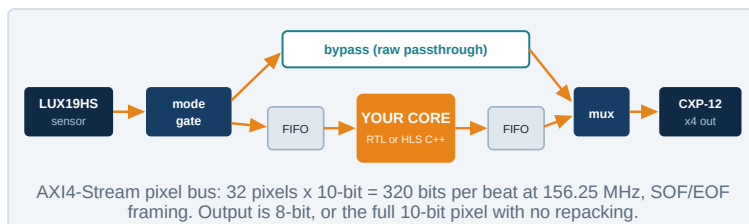
1920 X 16, WINDOWED

1 command
ALGORITHM TO
FLASH IMAGE

WHY BUILD ON THE HDK

- **Drop-in compute socket.** Your core slots into a fixed, hardware-validated datapath: no block-design editing, no IP packaging, no firmware code. Copy a working example, write one JSON manifest, build.
- **Write it your way.** Native VHDL/Verilog at the full 320-bit sensor stream is the delivered flow; existing 8-bit streaming IP is reused *unmodified* (the HDK measures your core's AXI-Stream width and inserts a width/rate adapter automatically); an optional Vitis HLS flow covers C++.
- **Parameters become named GenICam features.** The manifest wires core parameters and status straight to GenICam features with meaningful names ([PixelGain](#), [FrameCount](#), ...): one feature write, live on the next clock. The GenICam XML, the firmware bindings, and the register-map docs are all generated from the same manifest, so they can never drift.
- **Switch processing live.** Runtime bypass/compute selection is frame-boundary safe while streaming, with no image shift: A/B your algorithm against the raw image without stopping acquisition.
- **Own the digital I/O.** Only the HDK gives your logic direct access to the camera's two digital inputs and two outputs - drive triggers, strobes, or real-time flags straight from your core.
- **Know it keeps up.** Six built-in hardware counters report frames, beats and stall cycles at the compute socket, so throughput is measured on the camera, not guessed.
- **Verify before you flash.** Self-checking full-chain simulation (image in, image out, bit-exact golden model, live mode switches), a structural design audit, and documented throughput-budgeting rules per core shape.

DATAPATH



Hardware-validated, not just simulated. The delivered native 320-bit RTL image and the HLS arm both stream the full sensor rate - 2,247 fps at 1920 x 1080 over CXP-12 x4, 8-bit output - with live parameter updates and a clean image, and the mode switch is shift-free. Throughput budgeting for narrow cores is documented per lane count.



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PLATFORM AT A GLANCE

Camera	GigaSens CV 2.0 CXP; CV20-M-2000-CXP (mono) / CV20-C-2000-CXP (color)
Interface	CoaXPress CXP-12 x4, GenICam control
Sensor	Luxima LUX19HS, 4/3" CMOS global shutter, 10-bit
Frame rates	2,247 fps @ 1920 x 1080, 8-bit out 1,798 fps @ 1920 x 1080, 10-bit out 109,418 fps @ 1920 x 16, 8-bit out
Pixel stream	AXI4-Stream, 32 px x 10-bit (320 b/beat) @ 156.25 MHz; 8-bit or full 10-bit output
FPGA headroom	1,600 DSP slices, 329 block RAMs, 160K LUTs for your core (Kintex US XCKU035)
Memory	2 GB on-board DRAM
Host control	Named GenICam features + 32-register user file
Build	Vivado + Vitis 2024.2; Linux or native Windows
Physical	C / F-Mount; 80 x 80 x 53 mm, 450 g; 11 W, 12-24 VDC
Deliverable	Complete Vivado project bundle with working example cores and sim benches

THREE WAYS IN

You have	The HDK gives you
VHDL / Verilog	The delivered flow: native 320-bit socket at the full sensor rate. Working example: a per-pixel gain core whose parameter is the GenICam PixelGain feature.
Existing 8-bit streaming IP	Drops in verbatim: the socket auto-inserts the width/rate adapter and regenerates framing. No changes to your core.
C++	Optional Vitis HLS flow in the same socket, parameters on AXI-Lite reached through a built-in register window and firmware helpers.

ALGORITHM TO CAMERA IN FOUR STEPS



THE REST IS ALREADY DONE

- Frame-safe mode gating, FIFOs, clocking and resets
- GenICam XML + firmware bindings + register-map docs, per build
- Simulation suite + structural design audit
- Flashing flow with post-flash checks
- Quick-start and architecture guides