

CEDA Hardware Development Kit v2.9

Put your image-processing algorithm inside the GigaSens CV 2.0 10GigE camera.
1920 x 1080 at 536 fps - processed before it ever hits the wire.

536 fps

1920 X 1080, VALIDATED

10 GigE

GIGE VISION / GENICAM

10-bit in

FULL SENSOR DEPTH TO
YOUR CORE; 8-BIT OUT

Kintex US

XCKU035 FPGA

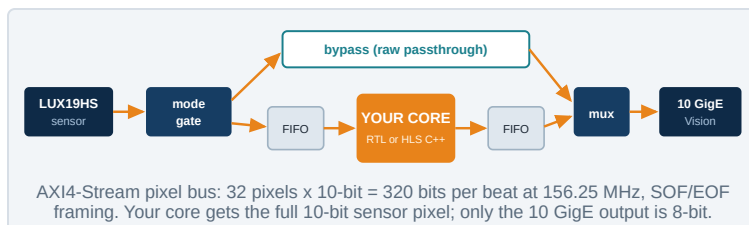
1 command

ALGORITHM TO
FLASH IMAGE

WHY BUILD ON THE HDK

- **Drop-in compute block.** Your core slots into a fixed, hardware-validated datapath: no block-design editing, no IP packaging, no firmware code. Copy a working example, write one JSON manifest, build.
- **Write it your way.** Native VHDL/Verilog at the full 320-bit sensor stream is the delivered flow; existing 8-bit streaming IP is reused *unmodified* (the HDK measures your core's AXI-Stream width and inserts a width/rate adapter automatically); an optional Vitis HLS flow covers C++.
- **Parameters become GenICam registers.** The manifest wires core parameters and status straight to GenICam user registers: one register write, live on the next clock. The GenICam XML and the register-map docs are generated from the same manifest, so they can never drift.
- **Switch processing live.** Runtime bypass/compute selection is frame-boundary safe while streaming, with no image shift: A/B your algorithm against the raw image without stopping acquisition.
- **Own the digital I/O.** Only the HDK gives your logic direct access to the camera's two digital inputs and two outputs - drive triggers, strobes, or real-time flags straight from your core.
- **Know it keeps up.** Six built-in hardware counters report frames, beats and stall cycles at the compute slot, so throughput is measured on the camera, not guessed.
- **Verify before you flash.** Self-checking full-chain simulation (image in, image out, bit-exact golden model, live mode switches), a structural design audit, and documented throughput-budgeting rules per core shape.

DATAPATH



Hardware-validated, not just simulated. All three core shapes - native 320-bit RTL, width-adapted 8-bit RTL, and HLS C++ - are confirmed on the camera at full 1920 x 1080 @ 536 fps, with the mode switch shift-free and the measured throughput envelope documented per core shape and lane count.

PLATFORM AT A GLANCE

Camera	GigaSens CV 2.0 10GigE (CV20-M-2000-10G), 10GigE Vision
Interface	10 GigE Vision, GenICam control
Sensor	Luxima LUX19HS, 4/3" CMOS global shutter, 10-bit
Frame rates	536 fps @ 1920 x 1080 (full resolution, 8-bit out, validated); higher at reduced ROI
Pixel stream	AXI4-Stream, 32 px x 10-bit (320 b/beat) @ 156.25 MHz; full 10-bit pixels to your core, 8-bit output
FPGA headroom	1,576 DSP slices, 302 block RAMs, 150K LUTs for your core (measured; Kintex US XCKU035)
Memory	8 GB on-board DDR4 DRAM
Host control	GenICam over 10 GbE; 32-bit user register file
Build	Vivado + Vitis 2024.2; Linux or native Windows
Physical	C / F-Mount; 80 x 80 x 53 mm, 450 g; 11 W, 12-24 VDC
Deliverable	Complete Vivado project bundle with working example cores and sim benches

THREE WAYS IN

You have	The HDK gives you
VHDL / Verilog	Native 320-bit slot at the full sensor rate. Working example: a per-pixel gain core whose parameter is a GenICam register.
Existing 8-bit streaming IP	Drops in verbatim: the compute block auto-inserts the width/rate adapter and regenerates framing. Working example: an off-the-shelf threshold core, unmodified.
C++	Vitis HLS core in the same slot, parameters on AXI-Lite reached through a built-in register window and firmware helpers.

ALGORITHM TO CAMERA IN FOUR STEPS



THE REST IS ALREADY DONE

- Frame-safe mode gating, FIFOs, clocking and resets
- GenICam XML + firmware bindings + register-map docs, per build
- Simulation suite + structural design audit
- Flashing flow with post-flash checks
- Quick-start and architecture guides



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